



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/092,874
Confirmation No. 9983
Filing Date March 5, 2002
Inventor..... Yoshiki Hishiro
Assignee..... Micron Technology, Inc.
Group Art Unit..... 2814
Examiner G. Peralta
Attorney's Docket No. MI22-1873
Customer No. 021567
Title: Methods Of Forming Semiconductor Constructions

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

To: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

From: David G. Latwesen (Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

The Examiner states that the primary reasons for allowance of the claims include a feature of "forming a semiconductor construction comprising forming a second layer comprising at least 50 weight % carbon over and physically against" a recited first layer. Applicant respectfully notes that, of the two allowed independent claims 19 and 29, only claim 19 recites that a second layer is formed over and physically against a recited first layer. Claim 29 is silent as to whether the recited second layer is formed physically against the recited first layer, and is allowable for its own recited features other than recitation of a second layer formed physically against a first layer.

The Examiner's statement of reasons for allowance also indicates that a primary reason for allowance of the claims includes exposure of a recited photoresist system to a developing solvent. Applicant respectfully notes that independent claim 19 recites exposure of a recited photoresist system to a developing solvent, and independent claim 29 does not contain such recitation. Claim 29 is allowable for its own recited features, other than exposure of a recited photoresist to developing solvent.

Dated: _____

1/28/04

Respectfully submitted,

By: _____



David G. Latwesen, Ph.D.
Reg. No. 38,533